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EXAMINER	
DILLER, JESSE DAVID	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,682	ELBOIM ET AL.	
	Examiner	Art Unit	
	JESSE DILLER	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13,15-19,24 and 25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-13,15-19,24 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Examiner acknowledges receipt of the amendment in response to the office action dated 05/14/2008, which amendment was received 08/14/2008. At this point, claims 8 and 11 have been amended, claims 1-7, 14, 20-23 have been cancelled. Thus, claims 8-13, 15-19, 24-25 are now pending in the application.

Claim Rejections – 35 USC § 112 and 102

2. In response to their cancellation, the 35 USC § 102/103 rejections of claims 1-4, 6-7, and 20-21 are withdrawn.

Response to Arguments

3. Applicant's arguments filed with respect to the rejection of claims 8, 11 have been fully considered but they are not persuasive.

4. First, Applicants state that these claims are rejected by Kao in view of Bonaccio and Tomashima; note that this is incorrect. The claims were rejected by Bonaccio in view of Kao and Tomashima. This difference may clarify the rejection for the Applicant.

5. Applicants generally contend that the references do not teach the limitations of the claims; however, the arguments on pages 5-6 appear to be a general allegation of unpatentability. Which elements of the claims are Applicants alleging each particular

reference does not teach? The prior rejection clearly stated the sections of the references which teach the claim limitations.

6. Applicants also argue that the present invention provides benefits not taught by the references. In response, it is noted that these features upon which applicant relies (i.e., lower cost, less memory requirements) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

7. Applicants further argue that Tomashima is not analogous art to Bonaccio and Kao, that Bonaccio and Kao teach configuration data stored in BIOS and used for programming configuration registers, while Tomashima is directed to communications channel skew. However, Bonaccio states that "the invention finds application relative to practically any IC configured by registers, and accordingly, the teachings…should not be limited to a particular application" (Par. 20); Kao teaches similarly on Col. 7, lines 37-45. Tomashima is directed to configuring a memory for correct/optimum operation; Kao and Bonaccio are also directed to configuration systems. Therefore, while the three systems may not be in the precise same art area, they are directed to the same problem solving area, that of initializing/configuring memory systems for proper communication / operation.

8. Applicants traverse the OFFICIAL NOTICE and request citation of a reference to support the claim of obviousness. Therefore, references are included in the rejection

below; Several further references are included on the attached PTO-892, which deal with this kind of operation.

9. Finally, Applicants state that the art does not teach testing prior to manufacture; However, any testing on physical objects must necessarily include some manufacture (i.e., a prototype or other working element); therefore, there is no restriction against the prior art systems being such a prototype.

10. Therefore, the rejections are deemed proper.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 8-13, 15-19, 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bonaccio in view of Kao, Tomashima, and the Electronicstalk editorial team, in "Prototype Validation is Key to Working Silicon", hereinafter Electronicstalk.

9. As for claims 8, Bonaccio discloses:

- resetting each of the plurality of registers of a test device (100, Fig. 2) to a register default data value (Par. 6);
- loading the plurality of registers (Par. 32) according to the test information stored in a NV test memory (Par. 29, Fig. 1; the configuration sets are test information associated with various configurations);

10. Bonaccio does not expressly disclose that

- the test information includes a plurality of test address information and a plurality of test data corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written; or

11. Instead, Bonaccio teaches that the configuration sets stored in the non-volatile memory contain only data; an address generator, a start register, and a duration register (144, 150B, 150C, Fig. 2) are used to generate the addresses which correspond to the data and to the target register.

12. Kao discloses a similar system and method of loading configuration registers, where initialization data is stored in a non-volatile memory and subsequently loaded into the registers during system startup. In the system of Kao, an address generator is not used. Instead, the register address is stored in the memory along with the data to =be stored. See Fig. 5.

13. Bonaccio and Kao are analogous art because they are from the same area of endeavor, namely systems for loading configuration registers.

14. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Bonaccio by replacing the address generator and address registers 150b,c with the address+data system of Kao.

15. The motivation for doing so is taught by Kao on Col. 3, lines 9-15, namely that this increases system efficiency and speed. Because the address is already stored in the memory, the address generator does not need to generate an address; it can simply be loaded with the data.

16. Therefore, it would have been obvious to combine Kao with Bonaccio for the benefit of increased circuit simplicity and speed.

17. Bonaccio also does not expressly teach:

- further comprising repeating the resetting and loading at least three times to repeat a multi-stage test data loading process with subsequent test information stored in the non-volatile memory during a memory design validation stage; or
- the process is done during a memory design validation stage.

18. Tomashima teaches a system for synchronization and setup of memory devices. In this system, several variables are tested, delay and Vref (see Fig. 43). Multiple series of tests are run. Delay and Vref are initialized (to a default value) and the configuration tested (s4). If the test is successful, that is one item of test data having default value equal to desired data. In that case, an additional subset of the test data (Vref) is identified S6 and the test run again with a different value.

19. Tomashima and the system of Kao and Bonaccio are analogous art because they are from the same area of endeavor, namely memory system configuration.

20. At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the method of Tomashima in the system of Kao and Bonaccio for memory validation. Such a combination, recognizing that certain default values - while operable - are not optimal, would be motivated to retry the reset/loading/identifying process multiple (i.e., >3) times with different values in order to obtain optimal operation (see Tomashima, Col. 37, lines 25-30).

21. Therefore, it would have been obvious to combine Tomashima and the system of Kao and Bonaccio as above.

22. The system also does not expressly teach manufacturing a plurality of products based on the test information.

23. However, **Electronicstalk teaches** that upon successful validation of a test article, a plurality of products may be manufactured based on the test data (see page 2, pars 5-6).

24. Therefore, one of ordinary skill, having combined the systems of Tomashima, Kao, and Bonaccio as above, would be motivated to use the test information which results to manufacture products, thereby obtaining the invention as claimed in claim 8.

25. As for claim 9, Bonaccio also teaches:

- The loading occurs during the initialization of a communication controller device (see Par. 20; the IC is a HDD read channel controller, which is a communication controller device).

26. As for claim 10, Bonaccio teaches:

- updating the information stored in the non-volatile memory with a second plurality of address information and second a plurality of data corresponding to the second plurality of address information, each of the second plurality of address information identifying at least one of the plurality of to which a corresponding one of the second plurality of data should be written (The combination of par. 29 would allow the memory to store multiple data blocks; See Kao, Col. 7, lines 10-25).

27. As for claims 11, 15, Bonaccio discloses:

- selecting a desired configuration of a device, the desired configuration associated with desired data to be stored in a plurality of registers of the device;

(see Par. 9; also Par. 29, first 5 lines; also first half of Par. 27; the start register designates a configuration set)

- storing test information associated with the desired configuration in a memory (Par. 29, Fig. 1; the configuration sets are test information associated with various configurations);
- resetting each of the plurality of registers to a register default data value (Par. 6);
- loading at least two of the plurality of registers according to the test information (Par. 32),

28. Bonaccio does not expressly disclose that

- the test information includes a plurality of test address information and a plurality of test data corresponding to the plurality of test address information, each of the plurality of test address information identifying at least one of the plurality of registers to which a corresponding test data should be written; or

29. Instead, Bonaccio teaches that the configuration sets stored in the non-volatile memory contain only data; an address generator, a start register, and a duration register (144, 150B, 150C, Fig. 2) are used to generate the addresses which correspond to the data and to the target register.

30. **Kao discloses** a similar system and method of loading configuration registers, where initialization data is stored in a non-volatile memory and subsequently loaded into the registers during system startup. In the system of Kao, an address generator is not used. Instead, the register address is stored in the memory along with the data to =be stored. See Fig. 5.

31. Bonaccio and Kao are analogous art because they are from the same area of endeavor, namely systems for loading configuration registers.

32. At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Bonaccio by replacing the address generator and address registers 150b,c with the address+data system of Kao.

33. The motivation for doing so is taught by Kao on Col. 3, lines 9-15, namely that this increases system efficiency and speed. Because the address is already stored in the memory, the address generator does not need to generate an address; it can simply be loaded with the data.

34. Therefore, it would have been obvious to combine Kao with Bonaccio for the benefit of increased circuit simplicity and speed.

35. Bonaccio also does not expressly teach:

- identifying a subset of the plurality of test data that correspond to a subset of the plurality of registers having default data values equal to desired data for achieving the desired configuration *prior* to loading, and
- further comprising repeating the process, or that the process is done during a memory design validation stage.

36. Tomashima teaches a system for synchronization and setup of memory devices. In this system, several variables are tested, delay and Vref (see Fig. 43). Multiple series of tests are run. Delay and Vref are initialized (to a default value) and the configuration tested (s4). If the test is successful, that is one item of test data

having default value equal to desired data. In that case, an additional subset of the test data (Vref) is identified S6 and the test run again with a different value.

37. Tomashima and the system of Kao and Bonaccio are analogous art because they are from the same area of endeavor, namely memory system configuration.

38. At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the method of Tomashima in the system of Kao and Bonaccio for memory validation. Such a combination, recognizing that certain default values - while operable - are not optimal, would be motivated to retry the reset/loading/identifying process multiple (i.e., >3) times with different values in order to obtain optimal operation (see Tomashima, Col. 37, lines 25-30).

39. Therefore, it would have been obvious to combine Tomashima and the system of Kao and Bonaccio.

40. The system also does not expressly teach manufacturing a plurality of products based on the test information and the subset.

41. However, Electronicstalk teaches that upon successful validation of a test article, a plurality of products may be manufactured based on the test data (see page 2, pars 5-6).

42. Therefore, one of ordinary skill, having combined the systems of Tomashima, Kao, and Bonaccio as above, would be motivated to use the test information which results to manufacture products, thereby obtaining the invention as claimed in claim 11 and 15.

43. As for claim 12-13, the system of Bonaccio, Kao, and Tomashima further teaches:

- wherein the test information includes a word of register address information and corresponding register data words for each one of the plurality of registers (see Fig. 5, Kao; the test information includes a register address and corresponding data; see also Bonaccio, last half of Par. 23).

44. As for claim 16, the system of Bonaccio, Kao, and Tomashima teaches:

- resetting and loading occur during initialization of a communication controller device (see Bonaccio, ; Kao, Col. 3, lines 27-35: section b; the loading happens on startup).

45. As for claim 17, the system of Bonaccio, Kao, and Tomashima teaches:

- generating a desired information associated with the desired configuration, wherein generating comprises: if there exists at least one of the plurality of test data corresponding to one of the plurality of registers having default data values equal to desired data for achieving the desired configuration prior to loading, then, for at least 3 times, storing subsequent test information and repeating steps c), d), and e) using the subsequent test information; else identifying the desired information to be the test information. (see Tomashima, s4, s6-s7, Fig. 43. If the default vernier value is the correct one, as determined in step s1-s4 but the Vref is not max, then subsequent Vref values are utilized and the test is rerun (s7). Else, the desired information is set (s8); note that these steps may be repeated at least three times).

46. As for claim 18, the system of Bonaccio, Kao, and Tomashima teaches:

- Selecting a memory with a memory size less than or equal to a memory size sufficient to store the desired information (The memory has a size equal to a memory size sufficient to fill some or all the configuration registers; therefore it has a size equal to a size sufficient to store the information)

47. As for claim 19, the system of Bonaccio, Kao, and Tomashima teaches:

- Selecting a desired memory includes reducing a size of the memory to a size sufficient to store the subset of the plurality of these data and the corresponding test address information (see Bonaccio, Fig. 2: the size of the memory is sufficient to store the data).

48. As for claims 24-25, the system of Bonaccio, Kao, and Tomashima further teaches:

- repeating a multi-stage test data loading process, wherein repeating comprises storing subsequent test information and repeating c), d), and e) using the subsequent test information (note Tomashima, Fig. 43 and the discussion of Par. 35 above).

49. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kao in view of Bonaccio and Cohen, US 5,737,524 and Official Notice.

50. Kao teaches

- a plurality of test configuration registers of a device (210, Fig. 1),

- a non-volatile test memory storing information to load a plurality of configuration registers of a test device (160, Fig. 1), wherein
- the loading occurs during a memory design validation test (As noted in Par. 2, page 8 of the reply dated 10/23/06, the 'during a memory design validation stage' "is only to exclude normal operating mode". The process of Kao happens not in normal operating mode, but during a configuration mode. See Col. 2, lines 42-46), wherein
- the information includes a plurality of address information and a plurality of data corresponding to the plurality of address information (see address information 0, 5, 5m, 5n and data information 1-4, 6, 5m+1-5m+4, Fig. 5),
- each of the plurality of address information identifying at least one of the plurality of configuration registers to which a corresponding data should be written (see Fig. 5; the address information is an index referring to the appropriate register; see 365, Fig. 3).
- a block of test control logic coupled to the memory, the block of control logic to write the plurality of data to the plurality of configuration registers according to the plurality of address information (see 205, Fig. 2; for multiple logic blocks which control the loading).
- The non-volatile memory is an Electrically Erasable Programmable Read-only Memory (See Col. 3, line 43) and
- the non-volatile memory has a memory size less than a memory size sufficient to fill all the configuration registers (The memory has a size equal to a memory size

sufficient to fill some or all the configuration registers; see Col. 3, lines 10-15 and Claim 2. The memory storing configuration information (0-5n in Fig. 5) is sized in multiples of the configuration register size, so as to be sized in accordance with the amount of information to be written. Therefore, when the configuration writes less than all of the registers, the memory storing configuration information has a size less than a size sufficient to fill all the registers)

51. Kao does not expressly teach that the device is an Ethernet controller device, instead teaching a PCI/ISA bus bridge.

52. Cohen teaches a similar system for loading configuration registers of a PCI/peripheral bus interface (24, Fig. 2) from a non-volatile memory (12D, Fig. 2). Cohen teaches that the PCI bus bridge may be used to interface different devices to the bus, such as an Ethernet device or a SCSI interface (Col. 2, lines 6-10).

53. At the time of the present invention it would have been obvious to one of ordinary skill in the art to modify the system of Kao by using it in an Ethernet controller device.

54. The motivation for doing so is taught by Cohen, in Col. 2, lines 6-28, namely that different devices that use a PCI bus use different configuration register settings. It may be possible to reuse the bus interface chip if the configuration settings are reprogrammable; therefore, the system to load the registers from a reprogrammable memory is used. A further motivation is found in Bonaccio, which also teaches a similar system for loading configuration registers from an EEPROM. Bonaccio teaches in Par. 4 that using programmable registers is widely used in many ICs to allow the user to configure the function of the chip. Further, in Pars. 20-21, he teaches that the methods

of loading configuration registers (which are similar to those of the present invention) may be applied not only to ICs such as hard disk channel controllers, but to any IC configured by registers.

55. Therefore, one of ordinary skill would be motivated to use the system of Kao in an Ethernet device as does Cohen.

56. As for the 'in a test laboratory' limitation, this limitation is intended use and does not structurally differentiate the claim from the prior art; the system is capable of being used in a test laboratory, thereby obtaining the invention of claims 20-22.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Kim, et al., and Madge, et al.,** in their papers for the September 2003 periodical *IEEE Design & Test of Computers,* discuss methods for 'binning' memory articles, which is pertinent to the claims. Copies of these papers are attached hereto.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE DILLER whose telephone number is (571)272-4173. The examiner can normally be reached on 9:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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